AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Currently Amended) A display device, comprising:

a display panel on which pixels corresponding to respective intersections of row lines and column lines are provided in a matrix manner;

a row drive circuit which receives a row drive timing signal for driving the row lines of the display panel, and sequentially supplies row drive signals for driving the row lines to the respective row lines connected to the pixels, in accordance with the row drive timing signal;

a column drive circuit which receives display data and a column drive timing signal for driving the column lines of the display panel, and supplies column drive signals corresponding to the display data to the respective column lines connected to the pixels, in accordance with the column drive timing signal; and

a control device which receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and outputs the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and the clock signal and supplies the column drive timing signal to the column drive circuit, along with the display data,

wherein:

the control device generates the row drive timing signal with reference to a timing of inputting the data enable signal and supplies the row drive timing signal, which has been generate, to the row drive circuit, so that one of the row drive signals is supplied to a first output terminal of the row drive circuit during a period from the timing of inputting the data enable signal to a start of the column drive circuit outputting the column drive signals of a first horizontal period of one vertical period, and

the row drive timing signal includes: a pulse shifted start pulse signal for determining timings to serially output the row drive signals to respective row lines; and a shift clock signal for determining a timing to shift the start pulse signal ~~the control device generating the row drive timing signal with reference to a timing of inputting the data enable signal in order to cause one of the row drive signals to be supplied to a first output terminal of the row drive circuit, and then supplying the row drive timing signal, which has been generated, to the row drive circuit~~.

2. (Currently Amended) The display device as defined in claim 1, wherein~~, the row drive timing signal includes:~~

~~a start pulse signal which is a pulse shifted in the row drive circuit in order to determine timings to serially output the row drive signals to the respective row lines; and~~

~~a shift clock signal which determines a timing to shift the start pulse signal, and~~

the control device starts to generate the start pulse signal at the timing of inputting the data enable signal, and generates a first

clock of the shift clock signal which allows the row drive circuit to obtain the start pulse signal, in order to cause the first output terminal of the row drive circuit to receive said one of the row drive signals, when a ~~predetermined~~ number of clocks of the clock signal is counted from the timing of inputting.

3. (Currently Amended) The display device as defined in claim 1, wherein~~, the row drive timing signal includes:~~

~~a start pulse signal which is a pulse shifted in the row drive circuit in order to determine timings to serially output the row drive signals to the respective row lines; and~~

~~a shift clock signal which determines a timing to shift the start pulse signal,~~

the control device starts to generate the start pulse signal at the timing of inputting the data enable signal to the control device, a first clock of the shift clock signal is generated when a predetermined number of clocks of the clock signal is counted from the timing of inputting, and

the row drive circuit obtains the start pulse signal in accordance with the first clock of the shift clock signal, to cause said one of the row drive signals to be outputted to the first output terminal.

4. (Withdrawn) The display device as defined in claim 1, further comprising dummy lines each having a dummy pixel, which are provided before a first row line and after a last row line of the display panel, respectively.

5. (Withdrawn) The display device as defined in claim 2, wherein, the control device supplies a column drive start timing signal, which is the column

drive timing signal determining timings at which the column drive circuit outputs the column drive signals, to the column drive circuit during a horizontal return period after completion of inputting the display data for one horizontal period to the column drive circuit, and then supplies clocks after the first clock of the shift clock signal to the row drive circuit, in accordance with the column drive start timing signal.

6. (Withdrawn) The display device as defined in claim 2, wherein, the control device inputs clocks, which are after the first clock of the shift clock signal, to the row drive circuit, in order to cause all of the row lines to have an identical drive period.

7. (Withdrawn) The display device as defined in claim 1, wherein, the control device causes the display data, which has been supplied, to be delayed for said one horizontal period, and then supplies the display data, which has been delayed, to the column drive circuit.

8. (Withdrawn) The display device as defined in claim 1, wherein, the number of the row lines connected to the pixels effective for displaying is 1050, and the row drive circuit includes 4 driver ICs being cascaded, each of the driver ICs having 263 output terminals for outputting the row drive signals.

9. (Currently Amended) A display device, comprising:

a display panel on which pixels corresponding to respective intersections of row lines and column lines are provided in a matrix manner;

a row drive circuit which receives a row drive timing signal for driving the row lines of the display panel, and sequentially supplies row drive signals for driving the row lines to the respective row lines connected to the pixels, in accordance with the row drive timing signal;

a column drive circuit which receives display data and a column drive timing signal for driving the column lines of the display panel, and supplies column drive signals corresponding to the display data to the respective column lines connected to the pixels, in accordance with the column drive timing signal; and

a control device which receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and outputs the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and the clock signal and supplies the column drive timing signal to the column drive circuit, along with the display data,

the control device including:

a start pulse signal generation section which starts to generate a start pulse signal which is a pulse shifted in the row drive circuit in order to determine timings to serially output the row drive signals, at the timing of inputting the data enable signal to the control device[[:]], and

a shift clock signal generation section which generates a first clock of a shift clock signal which determines a timing to shift the start pulse signal, when a predetermined number of clocks of the clock signal is counted from the timing of inputting the data enable signal, wherein

the row drive circuit ~~obtaining~~ obtains the start pulse signal in accordance with [[a]] the first clock of the shift clock

signal[[,]] so as to cause one of the row drive signals to be outputted to a first output terminal.

10. (Withdrawn) A display device, comprising:

a display panel on which pixels corresponding to respective intersections of row lines and column lines are provided in a matrix manner;

a row drive circuit which receives a row drive timing signal for driving the row lines of the display panel, and sequentially supplies row drive signals for driving the row lines to the respective row lines connected to the pixels, in accordance with the row drive timing signal;

a column drive circuit which receives display data and a column drive timing signal for driving the column lines of the display panel, and supplies column drive signals corresponding to the display data to the respective column lines connected to the pixels, in accordance with the column drive timing signal; and

a control device which receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and outputs the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and the clock signal and supplies the column drive timing signal to the column drive circuit, along with the display data,

the row drive circuit being arranged such that, driver ICs are disposed in accordance with a system-on-film structure, a line passing under an IC chip of predetermined one of the driver ICs is connected to an output terminal next to

an output terminal corresponding to a last one of the row lines of said predetermined one of the driver ICs, and the line passing under the IC chip is provided before a first one of the row lines provided on the display panel, acting as a dummy row line.

11. (Currently Amended) A control device of a display drive circuit, wherein,

the display drive circuit includes: a row drive circuit which receives a row drive timing signal which is for driving row lines of a display panel on which pixels corresponding to respective intersections of the row lines and column lines are provided in a matrix manner, and serially outputs row drive signals, which are for driving the row lines, to the respective row lines connected to the pixels, in accordance with the row drive timing signal; and a column drive circuit which receives display data and a column drive timing signal which is for driving the column lines of the display panel, and outputs column drive signals, which correspond to the display data, to the respective column lines connected to the pixels, in accordance with the column line drive timing signal,

the control device receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and supplies the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and supplies the <u>colum drive timing signal</u> ~~clock signal~~ to the column drive circuit, along with the display data[[,]]; [[and]]

~~during a period from the~~ the control device generates the row drive timing signal with reference to a timing of inputting the data enable signal and supplies the row drive timing signal, which has been generated, to the row drive circuit, so that ~~to a start of outputting the column drive signals of a first horizontal period of one vertical period, the control device generates the row drive timing signal with reference to a timing of inputting the data enable signal, in order to cause~~ one of the row drive signals [[to be]] is supplied to a first output terminal of the row drive circuit during a period from the timing of inputting the data enable signal to a start of the column drive circuit outputting the column drive signals of a first horizontal period of one vertical period; and~~, and then supplies the row drive timing signal, which has been generated, to the row drive circuit~~

the row drive timing signal includes: a pulse shifted start pulse signal for determining timings to serially output the row drive signals to respective row lines; and a shift clock signal for determining a timing to shift the start pulse signal.

12. (Currently Amended) A driving method of a display device, wherein:

the display device includes: a display panel on which pixels corresponding to respective intersections of row lines and column lines are provided in a matrix manner; a row drive circuit which receives a row drive timing signal for driving the row lines of the display panel, and sequentially supplies row drive signals for driving the row lines to the respective row lines

connected to the pixels, in accordance with the row drive timing signal; a column drive circuit which receives display data and a column drive timing signal for driving the column lines of the display panel, and supplies column drive signals corresponding to the display data to the respective column lines connected to the pixels, in accordance with the column drive timing signal; and a control device which receives the display data, a data enable signal, and a clock signal, generates the row drive timing signal from the data enable signal and the clock signal and outputs the row drive timing signal to the row drive circuit, and generates the column drive timing signal from the data enable signal and the clock signal and supplies the column drive timing signal to the column drive circuit, along with the display data,

the display data, a data enable signal, and a clock signal are received, the row drive timing signal is generated from the data enable signal and the clock signal and supplied to the row drive circuit, and the column drive timing signal is generated from the data enable signal and the clock signal and supplied to the column drive circuit, along with the display data, and

the row drive timing signal is generated with reference to a timing of inputting the data enable signal and supplied to the row drive circuit, so that one of the row drive signals is supplied to a first output terminal of the row drive circuit during a period from the timing of inputting the data enable signal to a start of the column drive circuit outputting the column drive signals of a first horizontal period of one vertical period[[,]]; and

the row drive timing signal includes: a pulse shifted start pulse signal for determining timings to serially output the row drive signals to respective row lines; and a shift clock signal for determining a timing to shift the start pulse signal ~~is generated with reference to a timing of inputting the data enable signal, in order to cause one of the row drive signals to be supplied to a first output terminal of the row drive circuit, and then the row drive timing signal, which has been generated, is supplied to the row drive circuit~~.